AMD
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AMD coreboot Development
coreboot summit 2008

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April 3, 2008

Welcome!

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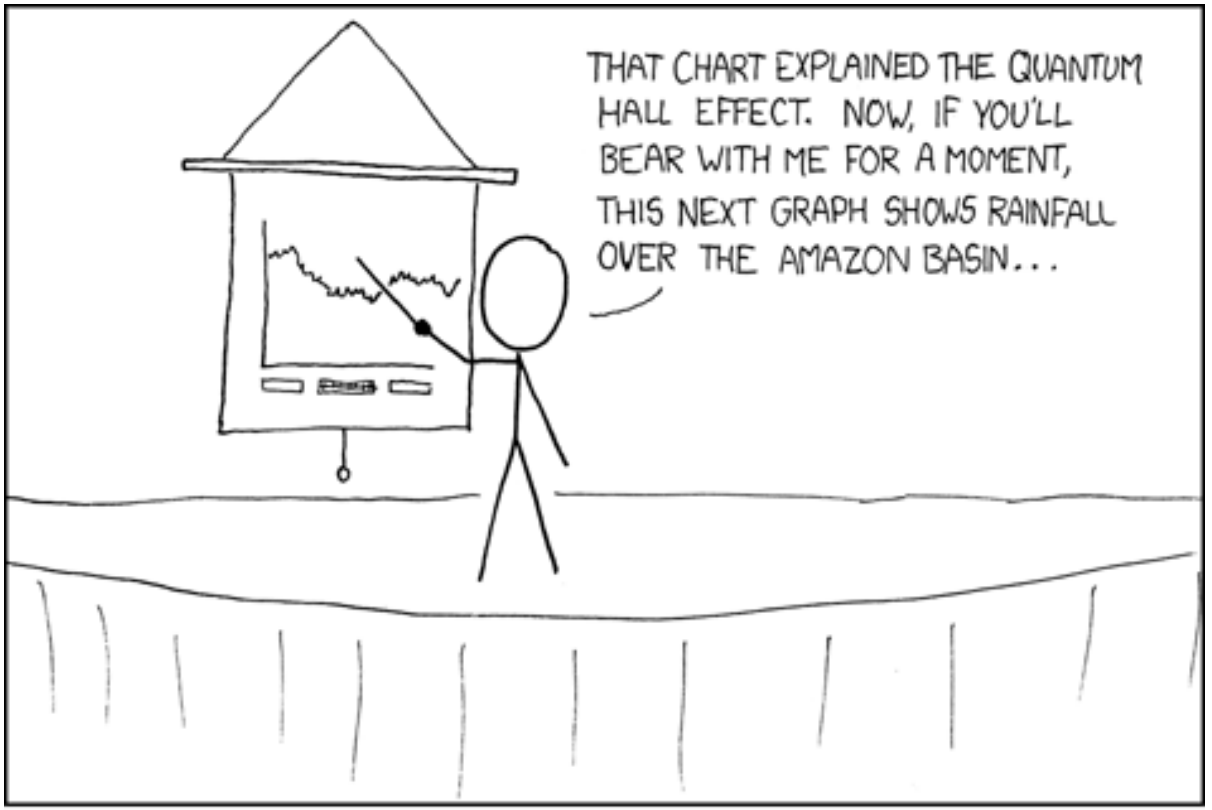

IF YOU KEEP SAYING "BEAR WITH ME FOR A MOMENT", PEOPLE TAKE A WHILE TO FIGURE OUT THAT YOU'RE JUST SHOWING THEM RANDOM SLIDES.

http://xkcd.com/365/

Overview

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coreboot features and capabilities align with AMD embedded development needs.

embedded == specialized applications and longevity

- low power compact systems
- high power headless systems

2007 Review

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- Geode™ LX support
  - V2 stability
  - V3 early development
- OLS 2007 presentation “Breaking the Chains”
  - http://coreboot.org/images/8/88/Crouse-Reprint.pdf
- buildrom improvements
- Family 10 support

Family 10 support

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- Port portions of AMD AGESA BIOS code
  - ~77,000 lines Microsoft® ASM and C code ported to ~26,000 lines of coreboot GCC C
    - code and comments
  - Checked in mid December

AGESA 3.x.y.z

- Supports rev F, rev G, and Barcelona
  - Only Barcelona ported
  - port rev F and rev G?
    - 1 coreboot to rule them all

AGESA ™

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AGESA = **A**MD **G**eneric **E**ncapsulated **S**oftware **A**rchitecture

- AGESA code is a generic encapsulation of AMD centric technology for the customer BIOS integration.
  - CPU Initialization
  - HT Initialization
  - Memory Initialization
- Simplified integration and easy maintenance
  - Not a binary module, compiled and linked with host BIOS.
- Timely updates
- Defined set of wrapper calls and callbacks.
- Rhymes with "a pizza"

Updating AGESA code is akin to replacing a puzzle piece with a new piece cut to the same exact shape.

AGESA – The Good

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- Same source as independent BIOS vendor (IBV) receive
- Tested by AMD and IBVs
- "automatic" configuration
- Performance and stability updates
- Regular releases
  - roadmap
- New CPU support

AGESA – The Bad

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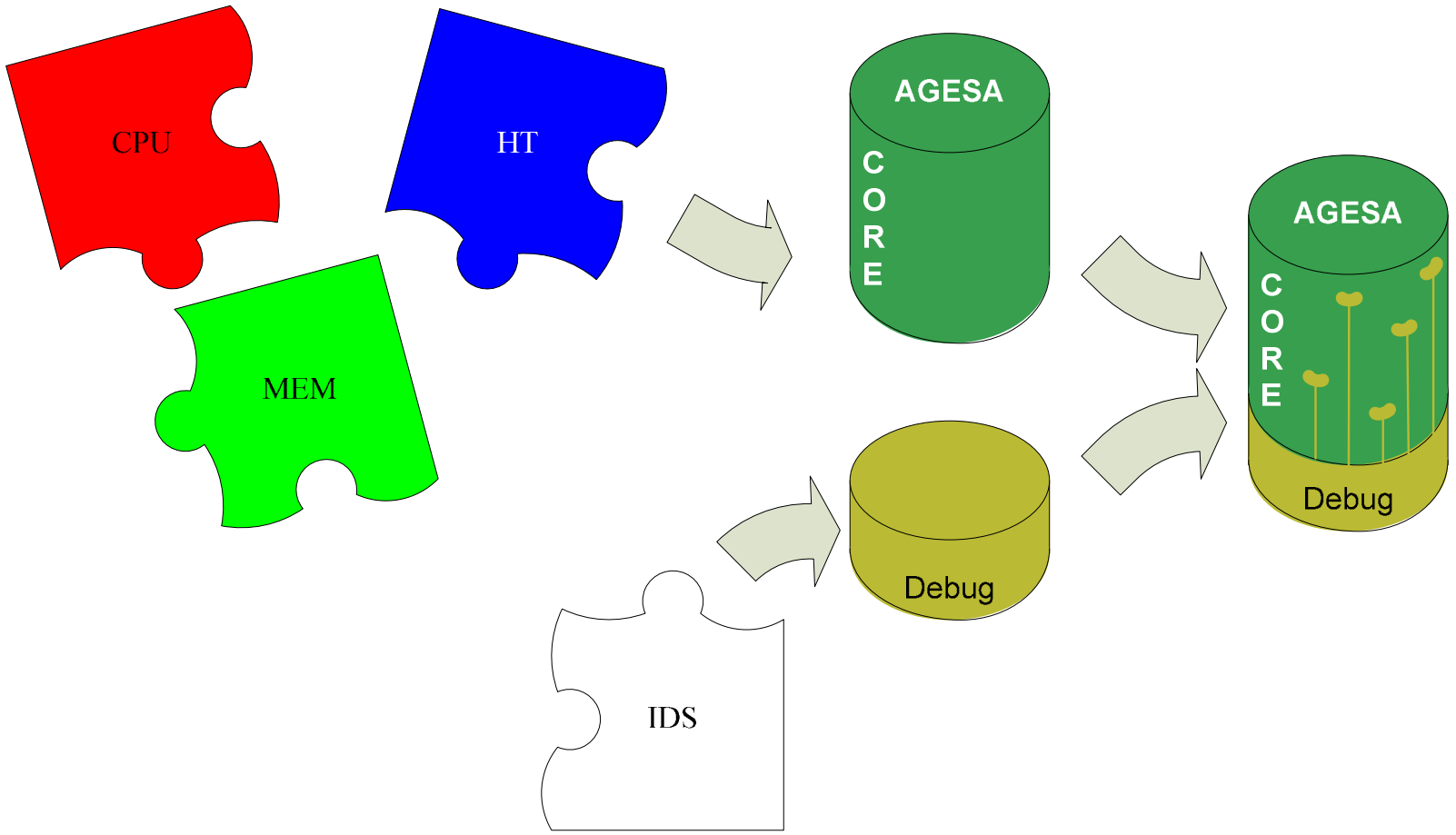
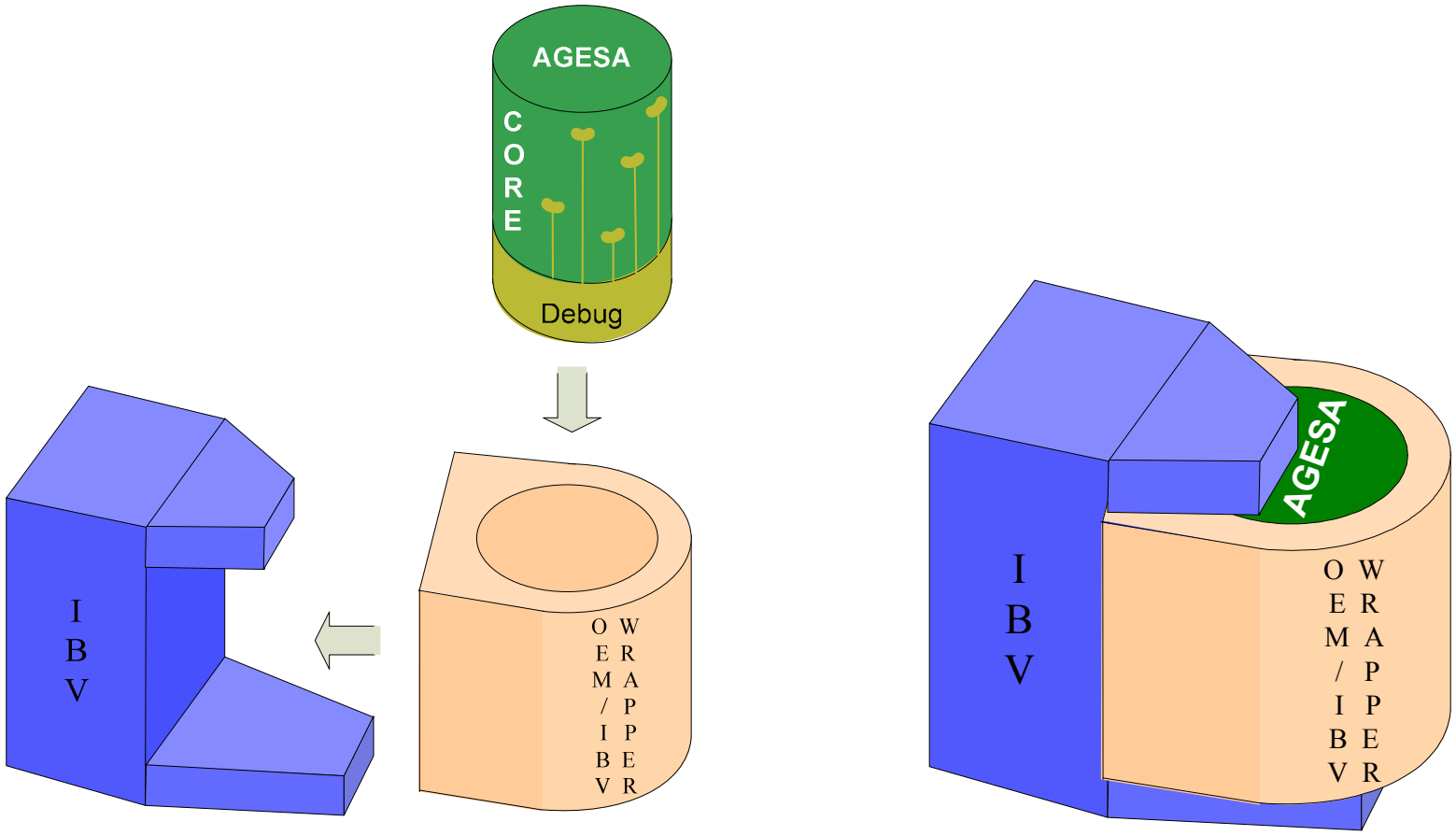
- Large and slow “automatic” setup
  - can be tuned
- Wrapper implementation
  - Even more code
- Complexity
  - Lots of configuration options
- AGESA structure vs. coreboot structure
  - CAR
  - Order of operations

AGESA Components



AGESA Wrapper



AGESA - Core Features

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Used by coreboot

- Advanced pre-memory environment
  - Cache as Stack (CAR)
  - Multi-processor communications
  - Parallel operations
- Hyper Transport coherent fabric initialization
- Initialization of all cores
  - BSP and all APs
  - APs left in halt state
- Memory controllers initialization and DIMM training

Not used by coreboot (yet)

- ACPI table generation
  - DSDT/SSDT entries for processors
  - SRAT
  - entries for WHEA tables (proposed)
- Legacy services:
  - Generate entries for SMBios tables (proposed)
- Integrated Debug support

AGESA - Core API (concepts)

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Minimal entry points

- Required parameters kept to a minimum
- coreboot more integrated

User options

- User selections in NVRAM

Call-Backs

- Used only when run-time calculations are required

AGESA v* (Future Versions)

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- All C and inline ASM
  - Less code to port to GCC
- flat mode
- improved APIs
- future CPU support
    - No K8 or Family 10
- dual license for IBVs and coreboot
  - release GPL v2 late 2008

AMD Southbridge (I/O) Support

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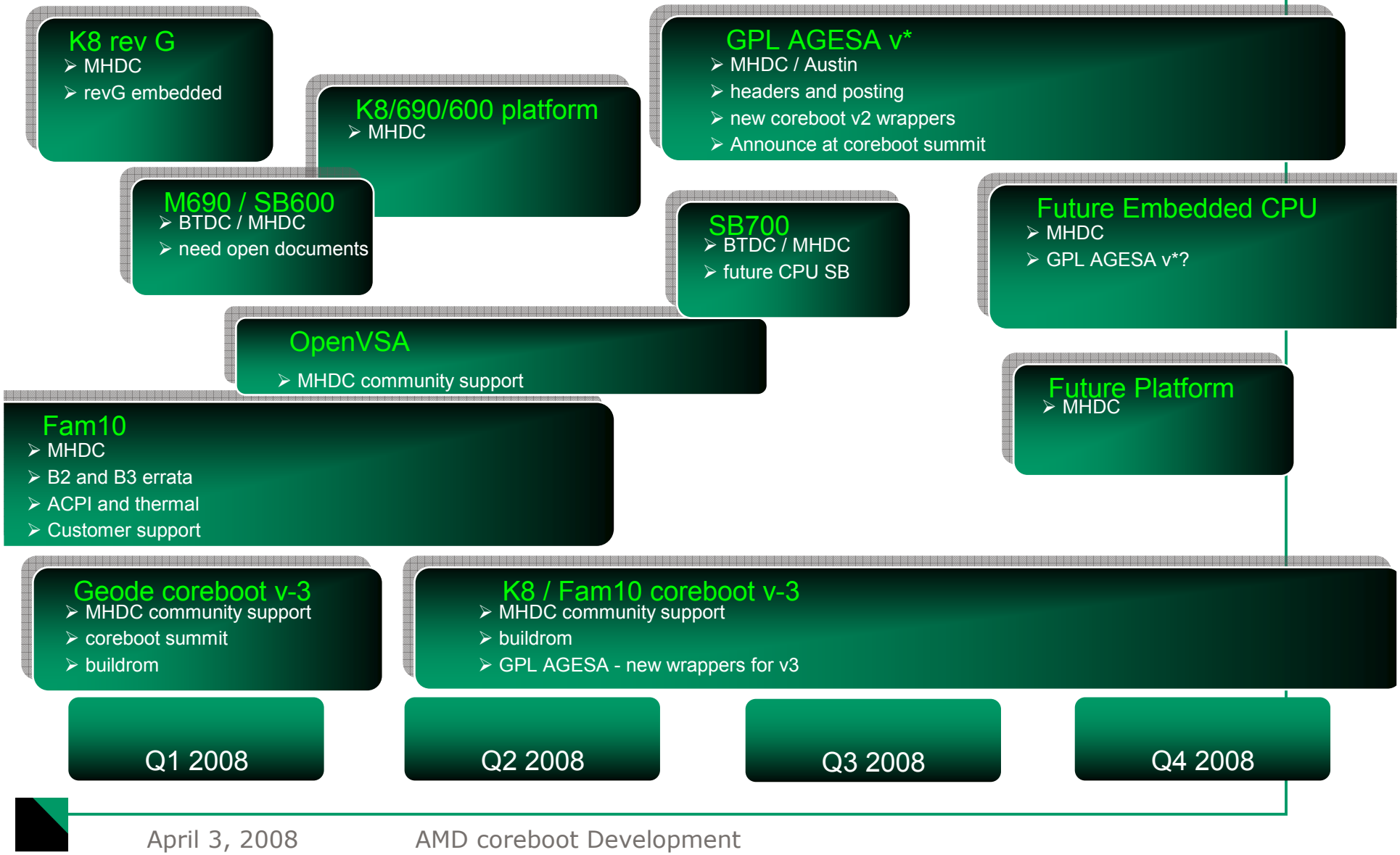
- Stable 8111/8131 support
- M690/SB600 support in May
- SB700 support mid to late 2008

- CIM-x southbridge source code
  - C code
  - Merge with AGESA
  - GPL?

AMD coreboot Roadmap



openVSA

- Port from Microsoft C bigreal to GCC flatmode
- it builds
- needs debug – stack segment issue
- svn @ coreboot.org

buildrom

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- Supports coreboot V2 and V3
- 13 platforms
- 7 payloads

SimNow™

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- Simulate AMD multi processor multi core systems
- Simulate AMD chipset 8111 family
- VGA and other peripherals
- Early development

AMD challenges

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- Changing the culture
- Source releases
  - Where and how
  - Multiple versions
- Document release
  - Processor documents
  - Chipset documents
  - Graphics documents

Improve coreboot

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- Commercial developer liaisons and support
  - OSS development process
  - Hit and run code drops
  - Culture and language differences
- Block owners
  - Cohesive structure and coding style
  - mainboard, CPU, northbridge, southbridge, PCI, config and make, etc…
- Development plan
  - Block owner meetings, irc, phone, summits
  - Roadmap; what, not when
  - Communication from core team is key
- Bug tracking
  - Bugzilla?
  - Feature requests?

Improve coreboot continued

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- Testing/QA
  - Is it any good?
  - Performance
    - Boot time
    - System settings
    - 3rd party testing – power-users
- ACPI
  - System description – MPTables, etc
  - power and temperature
- coreboot promotion
  - Commercial partners
  - OSS community

Improve coreboot continued

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- Tool chain
  - Recommendation
  - Range of versions
  - Stable vs. beta vs. alpha
- Small, simple and fast vs. full featured
  - OS requirements

Thank You!

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Thank you Ron, Stefan, Carl-Daniel, Uwe, Ward, Myles, and all the other coreboot developers!

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